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13. ABSTRACT (Maximum 200 words)

This project has explored possibilities for realizing a Kane-type quantum computer based on Si:P donor qubits. The overall goal has been to create an integrated process based on STM patterning of individual P-donor qubits, combined with single-electron transistors (SETs) for singlet-triplet spin state detection in the same lithographic step. The main accomplishments during this period have been to: (1) develop processes for positioning P atom donors and self-ordered arrays with near-atomic accuracy inside the silicon crystal lattice, (2) fabricate P donor nanowires as a major step toward an integrated epitaxial single-electron transistor, (3) measure electrical characteristics of the unpatterned P δ-layer and P donor nanowires, (4) compare the electrical data with our band structure calculations on the P δ-layer and previous theories of weak localization, (5) propose a new Kane-type architecture employing the idea of 'universal exchange' based on composite 3-electron spin qubits, and (6) perform extensive simulations to confirm the fundamental aspects of this approach, and quantify major difficulties to be overcome. Sustained effort in these directions will be required to realize a working qubit.

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Statement of the problem studied

This project has explored possibilities for realizing a Kane-type quantum computer based on Si:P donor qubits. We previously developed atom-resolved STM e-beam lithography to remove hydrogen from H-terminated silicon surfaces.[1] Our subsequent proposal to adsorb PH_3 precursor molecules selectively onto the STM-exposed Si dangling bonds, to be followed by low-temperature Si overgrowth,[2] was published in 1998 concurrent with Kane's paper[3]. This approach immediately became the 'bottom-up' strategy for building a silicon-based quantum computer using linear arrays of individual P-atom donors positioned into the Si crystal lattice with atomic accuracy for qubits.

Building a solid-state QC architecture of this type presents unprecedented challenges that take silicon-based electronics to its ultimate limits. Nevertheless, it can be argued that this approach is unique in its potential for scaling to levels of integration that could realize a useful quantum computer. Pursuit of this goal is a long-term proposition. Sustained support of this research could be expected to tell us whether a Si quantum computer is within reach, while simultaneously producing results that will be relevant to future advances in integrated circuit technology. Most of the basic issues involved in fabricating P donor qubits and manipulation of their quantum states have been addressed by this project over the last three years in the following areas. Much remains to be done.

(1) UHV-STM process development for patterning P donors and Si overgrowth:

Further refinements of this technique are needed to realize a scalable Si quantum computer.

(2) Characterizing the ultra-dense ~1/4ML P δ-layer:

This is the first step toward patterning epitaxial single-electron transistors (SETs) for spin state detection along with the individual P donor qubits, in the same lithographic step.

(3) Nanoscale device fabrication and electrical testing:

These results take us to the brink of experiments on integrated SETs and spin state detection.

(4) Proposal for a new Kane-type architecture based on 'universal exchange':

Extensive simulations were carried out to confirm the fundamental aspects of this approach, and quantify major difficulties to be overcome.

(5) Development of experimental equipment:

Building of a new UHV system designed to integrate STM and e-beam lithography for SET devices, and installation of a new He_3 refrigerator to test them.

Summary of the most important results

(1) UHV-STM process development

Low temperature Si surface preparation

Nanoscale processes require a low thermal budget. A long-standing problem in this area has been how to achieve an atomically clean and flat Si(100) surface without invoking high temperature (1250ºC) flashing. Our approach is to combine limited wet-chemical etching to remove the native oxide with UHV low-energy ion sputtering to remove carbon contamination. We find that room temperature 300eV Ar^+ ion bombardment at a fluence of $1x10^{17}cm^{-2}$ can remove nearly all carbon contamination; and a subsequent 650°C-5 min anneal recrystallizes the amorphized layer to produce an atomically clean and flat surface as shown in Fig. 1(a). This surface can then be H-terminated *in situ* to preserve these properties. Fig. 1(b) shows an electron-stimulated desorption line patterned by STM on such a surface. The vacancy defects caused by Ar bombardment form (dark) lines perpendicular to the underlying dimer rows after annealing. As far as we can tell, no adverse effects result from these vacancy-line defects in subsequent nanoscale device fabrication, because they are filled in during epitaxial Si overgrowth. This process has been carefully optimized to yield the best possible surface for STM P donor patterning on a pre-implanted substrate. Ion sputtering at elevated temperatures creates surface roughening and pit formation, requiring annealing temperatures higher than 700ºC to smooth them out. Insufficient annealing at lower temperature and/or shorter time creates surfaces with many small terraces. [4,5]

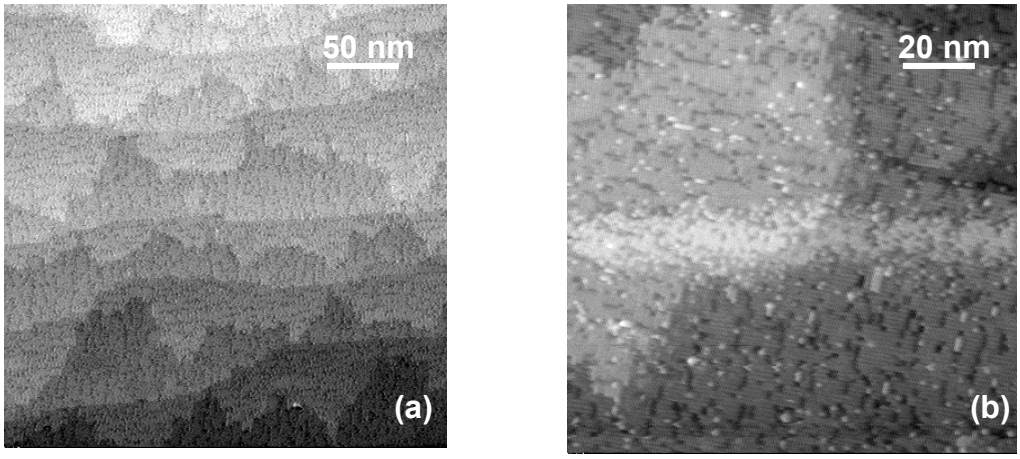


Figure 1 (a) A Si(100) surface cleaned by 300eV Ar ion sputtering followed by 650°C-5 min annealing. (b) A low-resolution Si dangling bond line patterned by STM in field emission mode on the H-terminated surface.

Phosphine dosing and silicon overgrowth

A great deal of effort has been devoted to developing the UHV processes for phosphine dosing and low-temperature Si overgrowth. Technical details may be found in our publications on this subject.[6,7] The optimal overgrowth technique has yet to be defined, however, because accurate measurements of P atom diffusion in the growth direction are not currently available on the atomic scale. Nevertheless, considerable progress has been made in this direction and options have been defined.

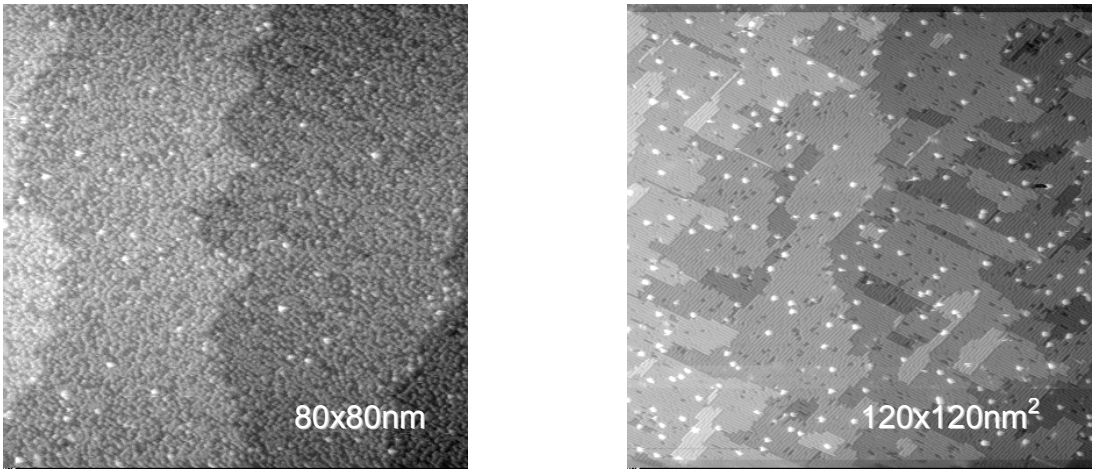


Figure 2 Atom-resolved STM images: (a) a UHV clean Si(001) surface dosed to saturation with PH_3 precursor molecules, and (b) the same sample following low-temperature Si overgrowth (bright spots are vacancies in the hydrogen termination applied to preserve the finished surface).

(2) <u>Characterizing the ultra-dense P δ-layer</u>

Hall effect and weak localization

Hall effect data on the unpatterned P δ-layer show a fully activated 2D electron gas up to ~$2x10^{14}cm^{-2}$ planar density, grown from a saturated ~0.2ML PH_3 precursor layer.[6,8] This unique 2D electron gas has properties very different from MOS inversion layers and modulation doped GaAs. Metallic conduction persists below 0.3K, and pronounced weak localization effects are observed similar to a 'dirty' metal film. The origin of this behavior is a rapid scattering rate for electrons confined tightly to the ultra-dense doping plane. This produces a multitude of closed diffusion loops that combine quantum mechanically with their time-reversed counterparts to increase resistance. An applied magnetic field reduces, and eventually eliminates, the resistive quantum interference effect of electron wavefunctions when a single flux quantum threads the area of a typical diffusion loop. Figure 3(a) illustrates the pronounced resistance peak at B=0 in magneto-transport data due to this effect. In Fig. 3(b), the same data is converted to changes in conductivity and compared to 2D weak localization theory. The result is an estimate of L ~ 150nm for the phase coherence length, over which diffusing electron

wavefunctions interfere before they suffer an *in*elastic collision. Compared to the ~2nm elastic mean-free path (inferred from conductivity), the phase coherence length in the P δ-layer is surprisingly long. Because these ultra-dense 2D donor sheets are grown into the silicon crystal lattice from molecular precursors that can be patterned by e-beam, they are likely to find important applications in a future nanotechnology.

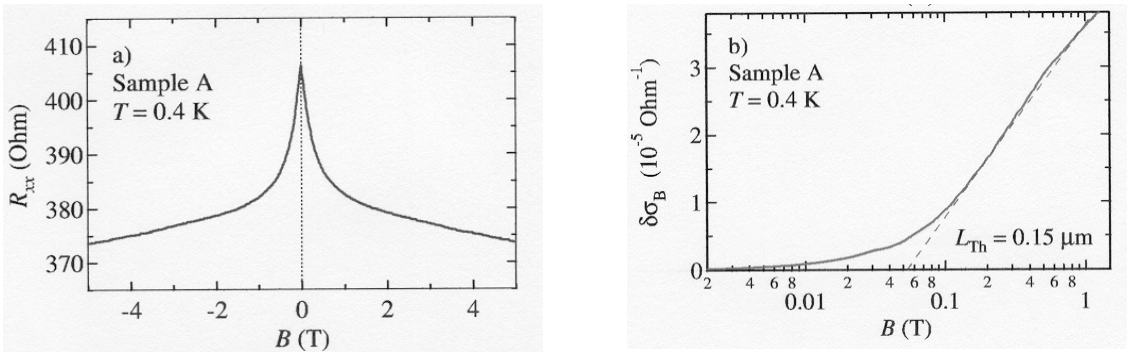


Figure 3 (a) Magneto-resistance data on the ultra-dense P δ-layer. (b) Fit of changes in conductivity to 2D weak localization theory.

Theoretical study of phosphorous δ-doped silicon

Because we intend to pattern single-electron transistors and other nanodevices using this process, a detailed understanding of the electronic band structure is required.

The average distance between donors in the saturated ~1/4ML δ-layer is ~0.8nm, much smaller than the first Bohr radius of ~2.3nm for an isolated P donor. This insures metallic conduction to ~0.3K and below. STM images show PH_3 precursor molecules are strongly self-ordered onto alternate sites along an individual dimer row of Si dangling bonds, and staggered between adjacent rows to form a ~1/4ML adlayer at saturation coverage with many localized regions of c(2x2) structure. For purposes of calculation, we employed an idealized c(2x2) planar lattice. Local variations in the exact position of each P donor causes scattering, but this will have very little effect on the 2D band structure.

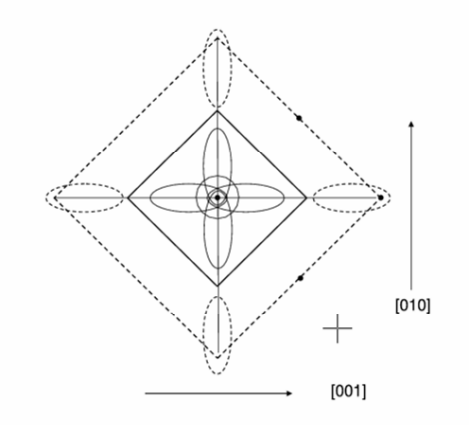


Figure 4. Schematic diagram of the 1x1 (dashed) and c(2x2) (solid) Brillouin zones for the Si(001) surface. Constant energy surfaces for the four in-plane valleys are projected into the smaller c(2x2) BZ, with circles representing the two +z and -z valleys at k=0.

Figure 5 illustrates our results for the P δ-layer subband structure.[9] Here the zero of energy is placed at the conduction band minimum of undoped Si far from the doping plane. Two sets of lines, dashed and solid, represent the calculation with and without the short-range interaction between electrons and donors. It was anticipated that this effect could be significant due to strong confinement at the doping plane, but we find this effect to play a relatively small role. Exchange-correlation, on the other hand, plays an important role that leads to a relatively large confinement potential of ~100meV at the Fermi level compared to the ~40meV binding energy of an isolated P donor.

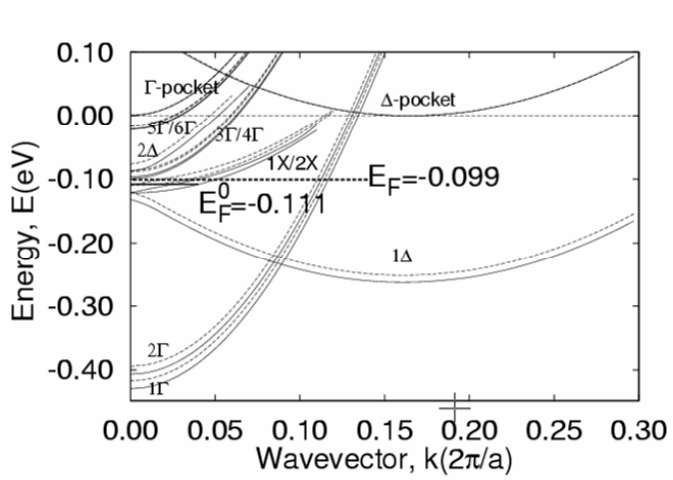


Figure 5. Subband structure for the idealized 1/4ML P δ-layer, k_x=0 to ~0.32π/a in the c(2x2) Brillouin zone.

Figure 6 illustrates the self-consistent potential of the 1/4ML P δ-layer vs. distance from the doping plane in the z (growth) direction. Solid lines show the calculated result including exchange-correlation, while dashed lines show the dramatic

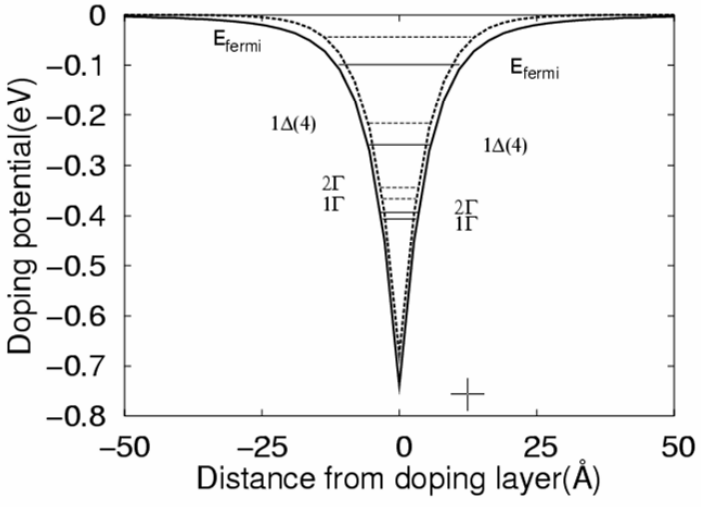


Figure 6. Self-consistent potential of the 1/4ML δ-layer, with lowest-lying subband energies included. Solid lines show the final result including exchange-correlation.

difference in binding energy without this interaction. The Fermi level is predicted to be ~100meV below the position of the conduction band edge farther than ~ 5nm from the dopant plane. Recent experimental evidence suggests that diffusion of P donors out of the plane may be as much as ~2nm for Si overgrowth at temperatures of ~250C,[10] but the resolution of these measurements is not sufficient to be definitive. This effect would, of course, widen the potential well shown here and reduce the binding energy. Although electrons may occupy one or more of the higher levels, the basic subband structure will remain and can be used as a guide to interpreting transport data.

(3) Nanoscale device fabrication and electrical testing

Ion-implanted contact arrays

Figure 7(a) shows a typical two-terminal device template with ion-implanted contacts and interdigitated lines. The individual lines are 0.8mm long and 1.3μm wide with 0.7μm spacing before annealing. The As^+ implant energy is 50keV, and dose is 0.5 to $1x10^{15}$ ions/cm^2. An atomic force microscopy (AFM) image is shown in Fig. 7(b). The resistance of individual implanted lines in test structures is ~20kΩ at 4K, which is within the expected range based on the implant/anneal parameters. The leakage resistance for the entire interdigitated array is typically in the GΩ range at 4K, provided the initial annealing temperature is not higher than 650ºC. The STM can therefore be positioned anywhere within the 0.8mmx0.8mm 'finger' region to pattern an nanoscale device between any pair of interdigitated contacts.[11]

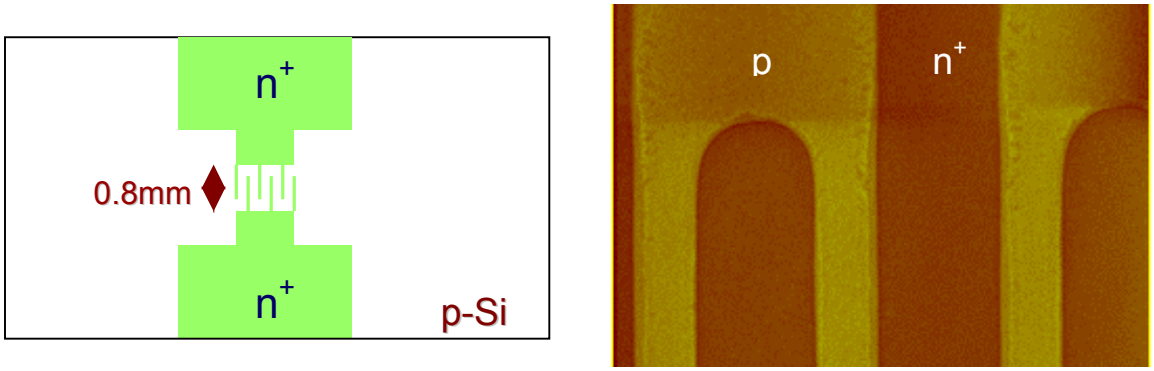


Figure 7 (a) Schematic of an ion implanted template. (b) AFM image after thermal annealing and HF etch, the As implanted fingers appear lower (darker).

Fabrication and testing of buried P donor nanowires

The first electrical devices of this kind are simple nanowires. Figure 8(a) shows one such nanowire after the STM lithography step. The bright ~33nm wide line of bare Si dangling bonds on the H-terminated Si(001) was created by multiple scanning of the STM tip at ~7V in field emission, across a 0.7μm wide gap between adjacent contact fingers. Immediately after this image was acquired, the sample was transferred to a

separate chamber and dosed with PH_3 to saturation. Finally, the sample was transferred again for epitaxial Si overgrowth to a thickness of ~3nm at very low temperature.

After removal from the UHV-STM system, In solder contacts were made to the large n+ implanted contact pads at top and bottom of the sketch in Fig. 7(a). The finished sample was then mounted onto a low-temperature probe, and electrical measurements were carried out in a liquid He_3 refrigerator. Figure 8(b) shows the I-V characteristics of three such samples. Continuous P donor nanowires have been tested down to ~10nm width, but below ~30nm it has been difficult obtain ohmic behavior at low bias---most likely due to a problem of continuity at the intersections between very small nanowires and the implanted finger contacts. Magneto-resistance measurements on wires of varying width show a dramatic difference in their weak localization behavior as the wire width becomes smaller than the phase coherence length.[11]

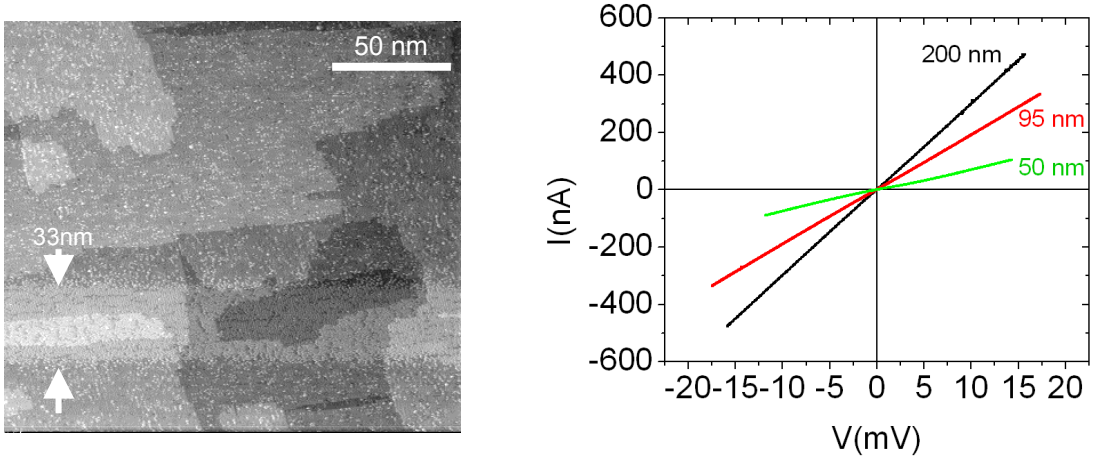


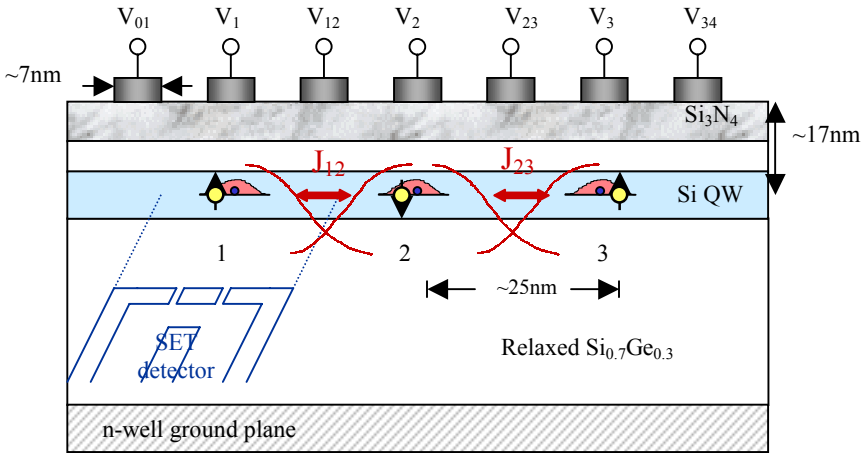
Figure 8 (a) atom-resolved STM image of a nanowire pattern after the STM lithography step to eliminate 'hydrogen resist', and prior to PH_3 dosing and Si overgrowth. (b) I-V characteristics for three finished nanowires of different widths at T=0.4K.

Successful fabrication of P donor nanowires represents an important step toward realizing epitaxial SETs that can be accurately positioned with respect to individual P atom qubits. Nanowires containing a ~10nm-wide gap are currently being fabricated for testing of planar tunnel junctions. We can now apply top-gates to these samples through a collaboration with Prof. T.-P. Ma's group at Yale. Thin SiNx dielectric films have been deposited onto our control samples at room temperature with good success, using the highly refined Jet Vapor Deposition (JVD) process. By this means, we should be able to modulate the potential barriers inside our nanowire gaps and characterize tunneling.

This part of the DARPA project is currently continuing under NSF NIRT sponsorship, at a substantially reduced funding level. Over the past year, this project has been delayed by the move of Prof. Du from the University of Utah to Rice University in Houston. We have now acquired our own LHe_3 refrigerator and installed it at Utah State University. It is up and running, and low temperature electrical measurements will resume shortly.

(4) Design and simulation of a new Kane architecture based on 'universal exchange'

The choice of architecture is crucial to a first demonstration of Si-based QC. DiVincenzo, et al.[12] have shown that nearest-neighbor Heisenberg exchange can be universal for composite 3-spin qubits; and this appears to offer the simplest possible implementation. Figure 9 illustrates our translation of this concept into a 3-P donor qubit with logic states encoded onto the S=1/2, S_z=1/2 subspace of the bound electrons.[13] Logic zero is represented by spins 1 and 2 in the singlet state S, and spin 3 up. Logic one is a linear combination of triplet states T_+ and T_0 for spins 1 and 2, with spin 3 down and up respectively, that preserves the overall spin quantum numbers. Initializing to logic zero is achieved by cooling the system in a large magnetic field to polarize spin 3, while inducing an even greater exchange coupling, $J_{initial}>2\mu_B B>>k_B T$, between spins 1 and 2 to produce the equilibrium spin singlet. Typical parameters for 10^{-6} initialization error at T=100mK are B~1T and $J_{initial}$~200μeV. In this electron-spin qubit, the hyperfine interaction with ^{31}P nuclei is suppressed by the large magnetic field, adding only a rapidly oscillating spin-flip component of order ~10^{-3} to electron wavefunctions outside the encoded subspace.



$$|0_L\rangle = |S\rangle|\uparrow\rangle \qquad |1_L\rangle = (2/3)^{1/2}|T_+\rangle|\downarrow\rangle - (1/3)^{1/2}|T_0\rangle|\uparrow\rangle$$

Figure 9. Composite 3-spin "universal exchange" qubit comprised of individual Si:P donor atoms in a Kane-type architecture with integrated SET readout patterned in the same lithographic step.

One-qubit operations are implemented with nearest-neighbor exchange in four or fewer steps, eliminating the need for gated ESR rotations. The two-qubit CNOT operation can also be performed by nearest-neighbor exchange within a 1D array, in 19 steps.[12] This large overhead for 'universal exchange' may not be optimal for a large-scale quantum computer, but the internal structure of the 3-spin qubit is uniquely suited to an initial demonstration. The most important property is the ability to perform a detailed calibration of exchange energies as a function of gate voltage before attempting high-frequency entanglement operations.[13]

In Fig. 9, the individual phosphorous donors are positioned ~25nm apart, and grown into the center of a strained Si quantum well on a relaxed $Si_{0.7}Ge_{0.3}$ substrate along with an SET for read-out. The heterolayer structure provides a ~300meV confinement potential for the P donor electrons, to prevent ionization when relatively large gate voltages are applied. Extensive simulations have been carried out on this silicon-based quantum computer architecture to assess prospects for a successful implementation.[14]

An in-plane expansion of the strained Si crystal lattice lifts the 6-valley degeneracy, leaving the two perpendicular z valleys lower in energy by ~100meV from which the low-lying bound states must be constructed. Figure 10 shows the calculated energies of the two lowest bound states of an individual P donor electron as a function of quantum well thickness, together with their splitting. The splitting approaches a limit of ~3meV for well widths greater than ~6nm. This splitting is much smaller than in unstrained Si, ~15meV, due to lifting of the 6-fold valley degeneracy.

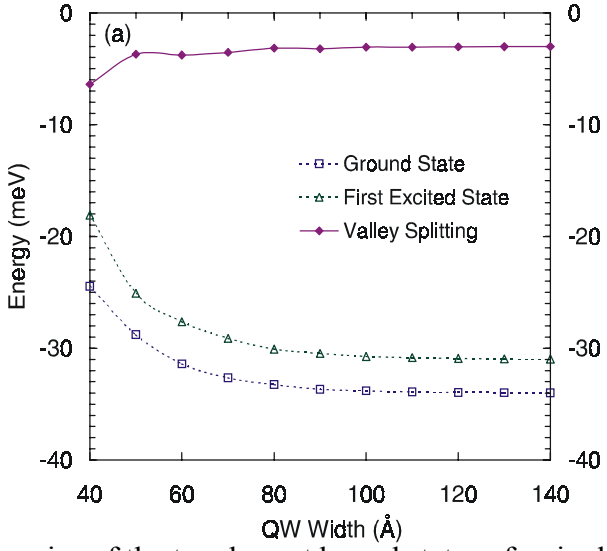


Figure 10. Energies of the two lowest bound states of a single Si:P donor at the center of a strained Si quantum well, as a function of well width.

The ground state is no longer spherically symmetric in the strained Si quantum well. The charge distribution normal to the plane oscillates with a period of $\pi/k_0 = 0.3$nm, but the unperturbed ground state electron remains localized within ~2-3nm of the P donor atom. Extensive simulations have been carried out to determine the effects of gate voltage on the exchange energy between electron ground states on nearest neighbor donors. To simplify the calculations, we consider a pair of coupled donors, labeled as 1 and 2 in Fig. 9, and assume that donor 3 is isolated. In this case, the exchange coupling is tunable via two gate voltages, the center voltage $V_c=V_{12}$ between the donors, and the outside confining voltages $V_g=V_{01}=V_{23}$. The gates directly above the donor atoms, V_1 and V_2, (known as A-gates) are disabled in our calculations, since they are not needed for tuning the exchange energy between a donor pair (they would, however, be required to help isolate the designated pair from adjacent electrons in the full array).

Figure 11 shows results representing two different bias conditions. The full-line potential curves are calculated at 17nm below the gate, corresponding to the center-line between the two donors. Two dashed lines characterize the gate-induced potential at 2nm above and below the donor plane. Panel (a) illustrates a reduction in the exchange energy between the two donor electrons. By applying a more positive voltage V_C to the center gate in panel (c), the exchange energy is enhanced. Potential contours of this type across the entire quantum well were then employed to calculate the self-consistent two-electron wavefunctions and evaluate the resulting exchange energy. By carrying out this procedure over a wide range of gate voltages, a much clearer indication of the possible performance of this architecture has emerged.[14]

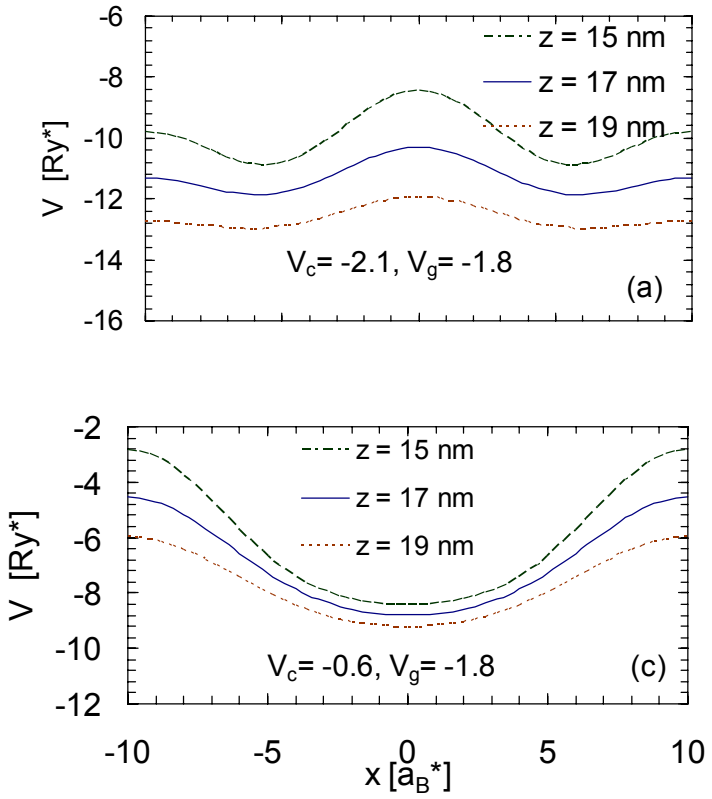


Figure 11. Gate-induced potential (in units of Ry*~30meV) for two sets of applied voltages. The individual P donors are placed at $5a_B$~12nm on either side of x=0.

Figure 12 shows a compilation of data for exchange energy J vs. center gate voltage V_C, for three values of voltage Vg on the outer gates. A single (violet) point at V_C=0 indicates the exchange energy of ~10^{-6} Ry* when no gate voltages are applied. Uniform exponential dependence on gate voltage V_C is predicted for all three values of the outside confining potential Vg over ~5 orders of magnitude. This result is an encouraging confirmation that the architecture shown in Fig. 9 is potentially viable. By examination of the data, we find that the range of exchange energies would be sufficient to initialize, calibrate, and implement quantum computation.

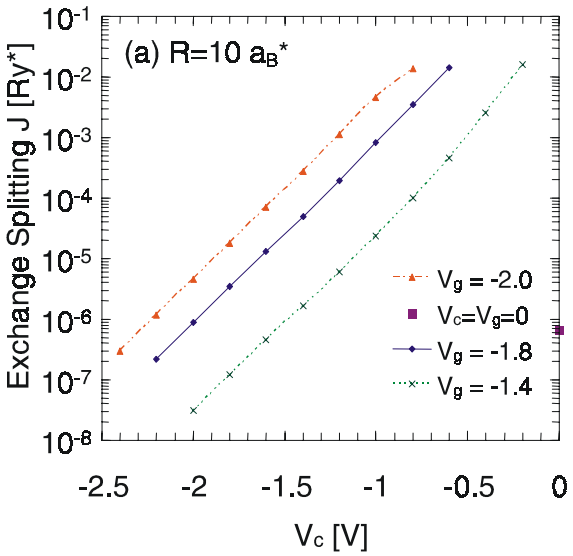


Figure 12. Exchange energy vs. center gate voltage V_C, for three values of Vg.

(5) <u>Development of experimental equipment</u>

New multi-chamber UHV-STM nanofabrication system

During the course of this project, a new multi-chamber UHV system was designed and built specifically for future research on integrated SET spin state detection. The main constituents are a sample preparation chamber, a STM chamber, and a chemical vapor deposition (CVD) chamber. The STM is built around a commercial RHK

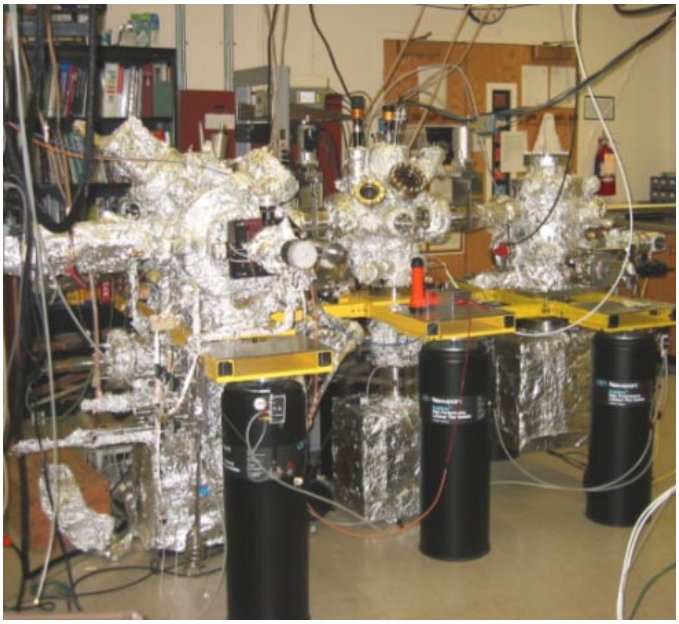


Figure 13. The new multiple-chamber UHV system at Utah State University.

model 300. The CVD chamber has the capability of exposing samples to a variety of gases from UHV to atmosphere. All chambers are equipped with independent pumping systems.

This system is capable of performing UHV-STM e-beam nanolithography with a range of 5μm, and epitaxial δ-layer growth with various dopants. The primary purpose of the new system will be to integrate our atom-scale device capability with state-of-the-art e-beam lithography at Lawrence Berkeley National Laboratory. Prof. Shen spent much of his sabbatical leave at LBNL last year. Integrated templates with registration marks have been designed, and they are now ready to be fabricated. The long-term goal is gate registration to P donor arrays.

Cryogenic system at USU

We have recently acquired a top-loading 0.3 -300 K cryostat with a 9T super-conducting magnet at to conduct transport studies of STM-defined nanodevices. The ^{4}He insert provides an ambient temperature of 1.4 -300 K while the ^{3}He insert provides 0.3-77 K. We have recently finished writing all of the LabView control software, and the system is now in operation.

Figure 14. The new low-temperature cryostat installed at Utah State University.

Listing of all publications and technical reports

(a) Published in journals

T.-C. Shen, J.-Y. Ji, M. A. Zudov, R.-R. Du, J. S. Kline, J. R. Tucker
"Ultradense phosphorous delta-layers grown into silicon from PH_3 molecular precursors",
Appl. Phys. Lett. 80, 1580 (2002).

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"Tunneling current through a quantum dot with strong electron-phonon interaction",
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"Effects of J-gate and uniform electric field on the exchange splitting of a coupled donor pair in Si for quantum computing"
Phys. Rev. B 66, 155331 (2002).

J. C. Kim, J.-Y. Ji, J. S. Kline, J. R. Tucker, T.-C. Shen
"Preparation of atomically clean and flat Si(100) surfaces by low-energy ion sputtering and low-temperature annealing"
Applied Surface Science 220, 293-297 (2003).

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"The role of antiphase boundaries during ion sputtering and solid phase epitaxy of Si(001)"
Surf. Sci. 538, L471 (2003).

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"Entanglement and correlation for identical particles in quantum computing"
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"A resonant spin lifetime transistor"
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David M.-T. Kuo, Y.-C. Chang
"Spontaneous emission spectrum of a single quantum dot embedded in a p-n junction"
Phys. Rev. B. in press, (2003).

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"The road to a silicon quantum computer"
Quantum Information and Computation, Vol. 3, Special, 105-113 (2004).

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J. R. Tucker
"Fabricating an all-epitaxial silicon quantum computer" (invited)
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Sydney, Australia, January 16-19, 2001.

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T.-C. Shen
"Low-temperature Si-MBE on Si(100) monohydride surfaces"
American Physical Society March Meeting, Seattle, March 13, 2001

T.-C. Shen
"From nanoscale to atom-scale devices: an opportunity for physicists"
Physics Colloquium, Arizona State University, Tempe, April 5, 2001.

T.-C. Shen
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T.-C. Shen
"Controlled coupling of donor atom-wavefunctions in silicon"
Quantum computing program review, Baltimore, Maryland, August 28, 2001.

T.-C. Shen
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Physics Colloquium, Utah State University, Logan, September 23, 2003.

T.-C. Shen
"Atom-scale devices based on 2D dopant patterns in silicon"
Nanotechnology seminar at ECE department, Purdue University, December 4, 2003.

T.-C. Shen
"Surface science, quantum transport and atom-scale electronics"
Physics Colloquium, Idaho State University, Pocatello, February 9, 2004.

T.-C. Shen
"Atom-scale electronics based on dopant patterns in silicon"
48th international conference on electron, ion and photon beam technology & nanofabrication, San Diego, June 4, 2004.

T.-C. Shen
"Two-dimensional dopant patterns as the building blocks for nanoelectronics"
Joint ACS 59th Northwest & 18th Rocky Mountain regional meeting, Utah State University, June 7, 2004.

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IEEE 2004 Silicon Nanoelectronics Workshop, Honolulu, HI, June 13-14, 2004.

T.-C. Shen
"Surface effects induced by B and As impurities in Si"
64th Physical Electronics Conference at University of California, Davis, California, June 23, 2004.

T.-C. Shen
"Nano- to atom-scale devices based on 2D donor patterns in silicon"
Solid state seminar, Yale University, New Heaven, September 21, 2004.

T.-C. Shen
"STM study of silicon surfaces at p-n junctions prepared by low-temperature processing"
51st International Symposium of AVS, Anaheim, CA, November17, 2004.

T.-C. Shen
"Integrable nano- to atom-scale 2D donor devices in silicon"
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Science and Technology colloquium, IBM Almaden Research Center at San Jose, California, June 24, 2005.

Y. C. Chang
"Simulation of Si:P qubit in realistic quantum computer architecture"
Invited talk, National Cheng-Kung University, Taiwan, July 28, 2005.

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Report of Inventions

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